GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

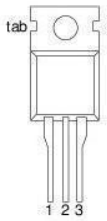
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
		500 500F 500G	**600 600F 600G**	**800 800F 800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	65	65	65	A

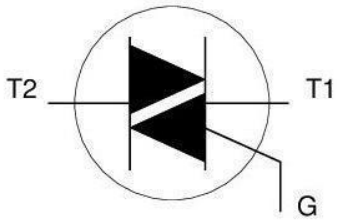
PINNING - TO220

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 102$ ˚C	-	8			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ ˚C prior to surge					
		t = 20 ms	-	65			A
		t = 16.7 ms	-	71			A
I^2t	I^2t for fusing	t = 10 ms	-	21			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 12 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	2.0	K/W
		half cycle	-	-	2.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
					...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
		T2- G+	-	30	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	30	30	45	mA
		T2+ G-	-	16	45	45	60	mA
		T2- G-	-	5	30	30	45	mA
		T2- G+	-	7	45	45	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	20	20	40	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
			...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 8 A; dI_{com}/dt = 3.6 A/ms; gate open circuit	-	-	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

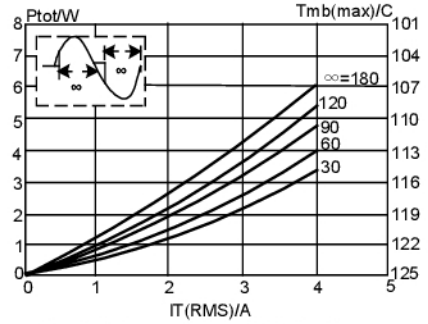


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

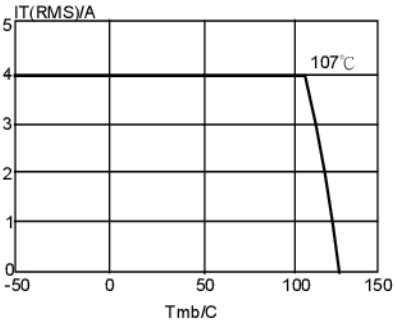


Fig.4. Maximum permissible rms current, $I_{T(RMS)}$, versus mounting base temperature T_{mb}

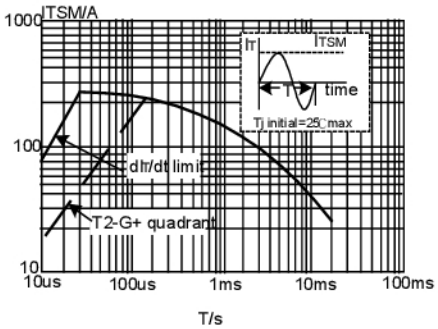


Fig.2.Maximum Permissible non-repetitive peak on-state Current I_{TSM}, versus pulse width t_p, for sinusoidal currents, t_p ≤ 20ms

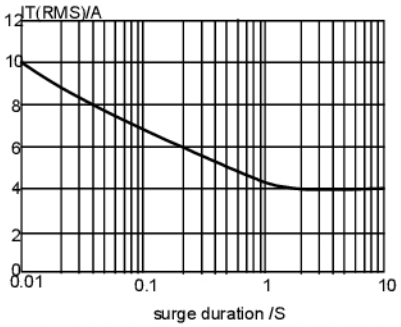


Fig. 5.Maximum permissible repetitive rms on-stat current $I_{T(RMS)}$ versus surge duration, for sinusoidal currents, f=50HZ; T_{mb} ≒ 107℃

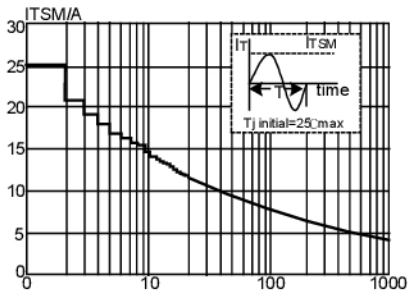


Fig3.Maximum Permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f=50HZ.

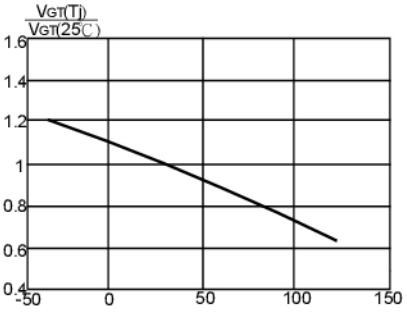


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25℃)$, versus junction temperature T_j

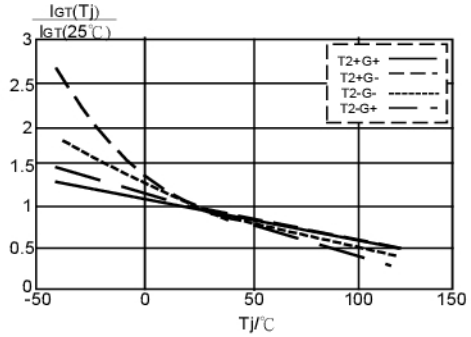


Fig. 7.Normalised gate trigger Current $I_{GT}(Tj)/I_{GT}(25℃)$,versus junction temperature Tj.

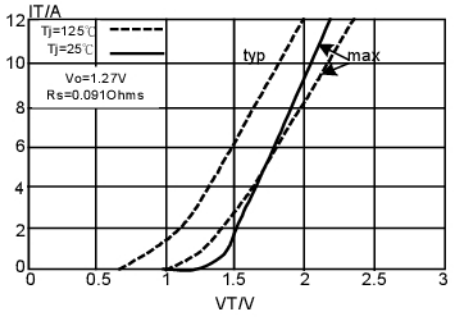


Fig.10.Typical and maximum on-state characteristic.

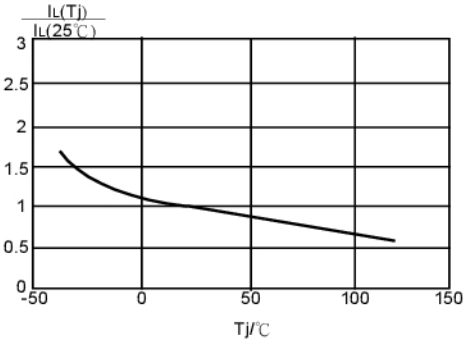


Fig.8.Normalised latching Current $I_L(Tj)/I_L(25℃)$, versus junction temperature Tj

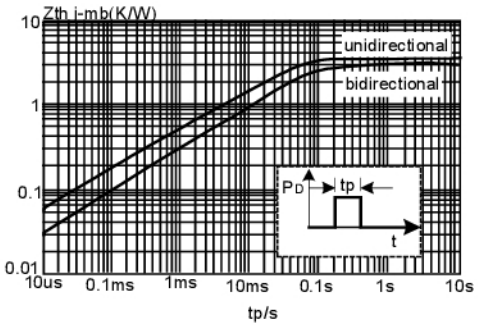


Fig.11.Transient thermal impedance Zthj-mb,versus pulse width tp.

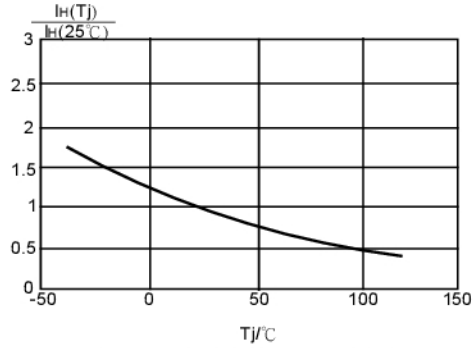


Fig. 9.Normalised holding current $I_H(Tj)/I_H(25℃)$, versus junction temperature Tj.

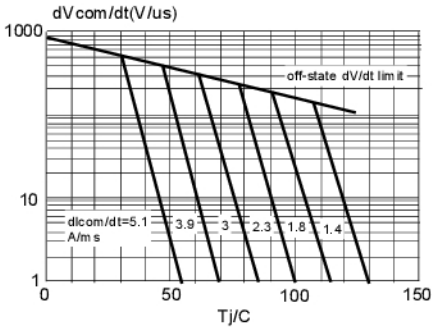


Fig.12.Typical commutation dV/dt versus junction temperature,parameter commutation dI_T/dt.The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt